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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BANANKHAH, MAJID A	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/606,839	KARDACH, JAMES P.	
	Examiner	Art Unit	
	Majid A. Banankhah	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This final action is in response to request for reconsideration filed on October 3, 2005. Application's argument has been fully considered but they not deemed to be persuasive. Claims 1-20 are considered for examination.

Response to Arguments

2. Applicant on page 7 of his remarks arguing that: "In order to establish a prima facie case of obviousness there must first be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, *the prior art reference (or references when combined) must teach or suggest all the claim limitations*." (Emphasis added). In re *Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Manual f Patent Examining Procedure (MPEP), 8tb Edition, Revision 2, May 2004, j2143. Applicant submits that there is no motivation to combine MacDonald, Simpson and Maupin.

In response, the Examiner has established a strong prima facie of obviousness and once a prima facie case of obviousness is established by Examiner, the burden shifts to applicants to rebut it with objective evidence of non-obviousness. E.g., In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). As noted by the Court of Customs and Patent Appeals, "argument cannot take the place of evidence." In re Langer, 503 F.2d 1380, 1395, 183 USPQ 288, 299 (CCPA 1974). In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). Applicants have not submitted sufficient evidence to rebut the strong prima facie case of obviousness established by Examiner. Regarding motivation, the Examiner has provided strong motivation why the references are combined and the motivation in the prior art to combine references does not have to be identical to that of the applicant to establish obviousness. In re Dillon, 919 F2d 688, 16 USPQ2d 1897 (Fed. Cir. 1990). Accord In re Kemps, --- F2d ---, --- USPQ2d --- (Fed Cir. 1996).

Applicant on page 8, argues that the CPU. Applicant submits that there is no motivation to combine MacDonald, Simpson and Maupin. As discussed above, the system in MacDonald is directed at handling real time interrupts in CPUS, Simpson relates to arbiter circuitry that is used to determine the priority level of various interrupts, and Maupin is a processor employing multiple sets of registers to eliminate interrupts. Applicant submits that it would not be obvious to combine the cited references since Maupin is eliminating interrupts, as opposed to generating them, while MacDonald and Simpson rely on the generation of interrupts. Because Maupin teaches away from MacDonald and Simpson, claim 1 is patentable over MacDonald in view of Simpson and further in view of Maupin.

Once again applicant is arguing the it would not be obvious to combine the references without providing any evidence as to why the references cannot be combined. As indicated in the previous office action, Maupin is used to show that it well known in the art to assign the high priority to real-time interrupt, for the reason that real time jobs do not miss their deadline and this is clearly indicated on column 7, lines 28-35. This is common sense and every priority system in the art of computer science reserves this option in order to efficiently meet their urgent tasks.

Applicant on page 9 further argues that: "Claim 7 recites a central processing unit (CPU) to generate a real-time interrupt upon receiving real-time analog data and to process data associated with the real-time interrupt if the real-time interrupt has a higher priority than a non-real-time operation currently being processed. Thus, for the reasons described above with respect to claim 1, claim 7 is also patentable over MacDonald in view of Simpson and further in view of Maupin. Since claims 8-12 and 19-20 depend on claim 7 and contain additional features, claims 8-12 and 19-20 are also patentable over MacDonald in view of Simpson and further in view of Maupin.

The system of Simpson explicitly teaches of "process data associated with the real-time interrupt if the real-time interrupt has a higher priority than a non-real-time operation currently being processed". Simpson explicitly teaches of this limitation. Simpson teaches of a method and means for handling multiple priority interrupt requests wherein arbitration circuit is provided for determining a priority status for each interrupt signal with the highest priority status and output circuitry, and an outputting circuitry, operable to output "an interrupt signal only in response to an interrupt signal having a higher priority status than any currently executing interrupt process" (see, Simpson (see, col. 1, lines 34-56). Regarding analog data, applicant's attention is directed to the teaching of Simpson on page 2, Col. 1, lines 5-13, where he define the "interrupt as being any action which causes the temporary cessation of execution by processor of a particular process so that the processor can execute an interrupt process. Such action is typically initiated in processor circuit by peripheral devices requesting the processor to interrupt execution of a main process to execute an interrupt process associated with that particular peripheral device". This system is not limited to real-time digital data to create real-time interrupt but covers both analog (created by a device) as well as digital data for creating real-time interrupt (See Simpson col. 1, lns. 6-13)

Claim 13 recites an event mechanism to generate real-time interrupts in response to receiving real-time data stored within a register, and an event handler to process data associated with the real-time interrupts received upon determining that relative priority between the real-time interrupts and non-real-time operations being processed. Thus, for the reasons described above with respect to claim 1, claim 13 is also patentable over MacDonald in view of Simpson and further in view of Maupin. Since claims 14-16 depend on claim 13 and contain additional features, claims 14-16 are also patentable over MacDonald in view of Simpson and further in view of Maupin.

The system of Simpson teaches of the detail of the interrupt handler in col. 3, lns. 23-37, where he teaches of the interrupt identifier that identifies an interrupt process for execution by the processor and correspond to a respective one of the interrupt signals.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-11, 13-15, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald (U.S. Pat. No. 6,295,574, hereinafter MacDonald) in view of Simpson (EP0742522A, hereinafter Simpson), and further in view of Maupin (U.S. Pat. No. 6,154,832, hereafter Maupin).

Per claim 1, teaches, Receiving a real time analog data (col. 5, lines 17-32, RT peripheral 114, data measured from a device) at a personal computer (Fig. 1, CPU 102) implementing a general purpose operating system (multi-tasking operating system, col. 1, lines 15-26), generating real time interrupt indicating a request to process real-time data at a central processing unit (col. 5, lines 33-54, interrupt service routine RTI peripheral 114, and processing time within the device cannot exceed the sample interval [real-time], CPU 102, see also, col. 3, lines 46-63); and

While the system of MacDonald suggesting the highest priority assignment to be given to real time interrupts but fails to teach of a step or means for determining the real time interrupts among the interrupts (real time and non real time). However, the reference of Simpson teaches of a method and means for handling multiple priority interrupt requests wherein arbitration circuit is provided for determining a priority status for each interrupt signal with the highest priority status and output circuitry, and an outputting circuitry, operable to output an interrupt signal only in response to an interrupt signal having a higher priority status than any currently executing interrupt process (see, Simpson (see, col. 1, lines 34-56).
processing the real-time event if the real time interrupt has a higher priority than the non real time operation (col. 1, lines 34-56). Non real time operation is any operation such as currently executing interrupt process in the above-cited paragraph.

Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use priority determination scheme of Simpson in the real time interrupt handling system of MacDonald, for the reason to be able to direct processors attention to high priority real time data than processing the less urgent or non real time data. Simpson suggests the motivation in col. 1, lines 22-29.

Additionally, the reference of McDonald in view of Simpson, does not clearly indicate that higher priority is assigned to real-time to real-time interrupts. However, Maupin explicitly teach of a system in which the processor includes an execution core configured to execute instructions and register file coupled to the execution core. The register file is divided into a plurality of register sets, and one of the pluralities of register sets is dedicated to a default task, and each remaining one of plurality of register sets is dedicated to different interrupt source (col. 2, lns. 56-64). Later Maupin teach that high priority be assigned to real-time interrupts (col. 7, lns. 21-35, the defined order may correspond to a priority scheme amongst the possible interrupt sources. For example, those interrupt sources which are "real-time" in nature (i.e. the interrupt source operates according to real-time as opposed to devices which may operate properly with any latency) may be defined as high priority while non-real-time interrupt sources may be lower priority. For example, video and audio devices are typically real-time devices.), for the reason not to delay real-time devices and cause a real time task wait while a non real time task is running. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to assign high priority to real time interrupts as opposed to non-real time interrupts.

As to claim 2, continuing processing the first event if the real-time event does not have a higher priority than the first process. In the system of Simpson, by default, when there is no higher priority interrupt than the currently running process (operation), the priority of the running process is higher and therefore, the process continue to run
without interruption (Simpson, Abstract, interrupt identifier is operable only in response to interrupt signals having a higher priority status than any currently executing interrupt process). Therefore, even though the interrupt is present, since the priority of the interrupt is not higher than the priority of the currently running process, the currently running task is not interrupted because the identifier circuit does not identify that.

Per claim 3, the context and state of the executing task is saved before the interrupt service routine is executed and the states are restored after execution of the real time [high priority] data is executed (see, MacDonald, col. 43-63, and col. 2, lines 18-39).

Per claims 4 and 5 are rejected for the reason explained in the rejection of claim 1. The method of Simpson, determine the priority among interrupts and make a determination as to which interrupt has the highest priority (see, Simpson, col. 1, lines 34-56). It is obvious that the processing will continue if the priority of the real time is not higher than the priority of the real time, because the arbiter looks at the priority and does not know whether the data is real time or not.

Per claim 6, the claim is rejected for the reasons stated in the rejection of claim 4, and the reference of Simpson further teaches of returning to execution of the interrupted process, meaning that the interrupted process is terminated when the arbiter receives a higher priority interrupt.

Per claim 7, a chipset (Fig. 1, 100), a bus coupled to the chipset (bus bridge 106); and a central processing unit (CPU), coupled to the bus (CPU 102), to generate a real time interrupt upon receiving real time analog data (col. 5, lines 33-54, interrupt service routine RTI peripheral 114, and processing time within the device cannot exceed the sample interval [real-time], CPU 102).

While the system of MacDonald suggesting the highest priority assignment to be given to real time interrupts fails to explicitly teach of processing data associated with real time interrupt "if the real time interrupt has a higher priority than a non real time operation currently being processed". However, the reference of Simpson explicitly teaches of this. Simpson teaches of a method and means for handling multiple priority interrupt requests wherein arbitration circuit is provided for determining a priority status for each interrupt signal with the highest priority status and output circuitry, and an outputting circuitry, operable to output "an interrupt signal only in response to an interrupt signal having a higher priority status than any currently executing interrupt process" (see, Simpson (see, col. 1, lines 34-56).
processing the real-time event if the real time interrupt has a higher priority than the non real time operation (col. 1, lines 34-56). Non real time operation is any operation such as currently executing interrupt process in the above-cited paragraph.

Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use priority determination scheme of Simpson in the real time interrupt handling system of MacDonald, for the reason to be able to direct processors attention to high priority real time data than processing the less urgent or non real time data. Simpson suggests the motivation in col. 1, lines 22-29.

Regarding analog data, applicant's attention is directed to the teaching of Simpson on page 2, Col. 1, lines 5-13, where he define the "interrupt as being any action which causes the temporary cessation of execution by processor of a particular process so that the processor can execute an interrupt process. Such action is typically initiated in processor circuit by peripheral devices requesting the processor to interrupt execution of a main process to execute an interrupt process associated with that particular peripheral device". This system is not limited to real-time digital data to create real-time interrupt but covers both analog (created by a device) as well as digital data for creating real-time interrupt (See Simpson col. 1, lns. 6-13).

Per claim 8, timer is inherent in an interrupt service routine disclosed in MacDonald (See also col. 3, lines 35-44, clock cycle), and generating real time interrupt is taught in col. 3, lines 46-63.

Per claim 9, processing real time interrupt is taught by MacDonald in col. 3, lines 46-63 (RTI), Simpson teaches of detail of an interrupt handler (see, Simpson col. 8, lines 9-42).

Per claim 10, register to store real time data is shown by MacDonald (see Abstract, registers allocated for real time use are indicated in the RTI register).

Per claim 11, as discussed in the rejection of claim 1, the reference of Simpson teaches of relative priority between real time interrupt and non real time operation.

Per claim 13, the claim is rejected for the reasons stated in the rejection of claims 8-10. Additionally, the detail of the interrupt handler is described by Simpson, as the interrupt identifier that identifies an interrupt process for execution by the processor and correspond to a respective one of the interrupt signals.

Per claims 14 and 20 using radio signal, as analog data does not modify the method of MacDonald, therefore, it is obvious to use radio signal as analog data if this is users desire.

Per claim 15, Simpson teaches of interrupt handler in col. 1, lines 34-65 (indication is held by storage circuitry and selecting the one interrupt signal with highest priority status).

Per claim 19 and generating real time interrupt in response to receiving timing signal from the timer is taught by MacDonald in col. 3, lines 46-63.

5. Claims 12, 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald (U.S. Pat. No. 6,295,574, hereinafter MacDonald) in view of Simpson (EP0742522A, hereinafter Simpson), in view of Maupin (U.S. Pat. No. 6,154,832, hereafter Maupin), and further in view of Williams et al. (U.S. Pat. No. 5,764,582).

It is noted that in the office action issued on June 30, 2005, due to a typographical error, the reference of Maupin is omitted from the title of the rejection in that section, however, since claims 12, and 16-18 are all dependent claims, it is clear that the claims are rejected under 35 USC 103 in view of the four cited references.

Per claims 12 and 16 the modified MacDonald fails to explicitly teach of analog to digital converter, However, the use of analog to digital converter is well known in the art as it is evidenced by Williams, in col. 4, lines 1-37 (D/A and A/D converters), for the reason to be able to process analog data and convert analog into digital. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to use Williams's analog to digital converter.

Per claim 17, registering is taught by MacDonald in the abstract, and col. 3, line 64 to col. 4, line 5.

Per claim 18, the timing signal is created by the clock cycle, and MacDonald teaches storing the interrupting the register in col. 3, lines 46-63.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Applicants amendment necessitated the new ground of rejection. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS

ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE The application has been amended as follows:
ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL

How to Contact the Examiner:

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Majid Banankhah, whose telephone number is 571-272-3770. A voice mail service is also available at this number. The Examiner can normally be reached on Monday, and Wednesday - Friday, 7:00 AM - 3:30 PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An Meng-Al who can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

All responses sent by U.S. Mail should be mailed to:

Commissioner for Patents
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Alexandria, VA 22313-1450

PTO CENTRAL FAX NUMBER:
703-872-9306

- any inquiry of a general nature or relating to the status of this Application should be directed to the TC 2100 Group receptionist: (703) 305-3900.

Majid Banankhah

MAJID BANANKHAH
PRIMARY EXAMINER

1/4/06